What is claimed is:

1. An improved memory structure comprising:

a memory structure, said memory structure comprising:

at least one memory cell structure;

at least one write word line operatively coupled to said at least one memory cell structure;

at least one read word line operatively coupled to said at least one memory cell structure;

at least one read bit line operatively coupled to said at least one memory cell structure; and

a corruption prevention circuit operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit forces said at least one read bit line to a known digital value.

2. The improved memory structure of Claim 1, wherein;

said known digital value is a digital low value.

3. The improved memory structure of Claim 2, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory

cell structure, said corruption prevention circuit causes said read bit line to be discharged.

4. The improved memory structure of Claim 1, wherein;

said memory structure is a rotated-read register file.

5. The improved memory structure of Claim 4, wherein;

said known digital value is a digital low value.

6. The improved memory structure of Claim 5, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

7. The improved memory structure of Claim 1, wherein;

said memory structure is a Content Addressable Memory array.

8. The improved memory structure of Claim 7, wherein;

said known digital value is a digital low value.

9. The improved memory structure of Claim 8, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

10. An improved memory structure comprising:

a memory structure, said memory structure comprising:

at least one memory cell structure, said at least one memory cell structure comprising:

a memory cell structure pull-down transistor, said memory cell structure pull-down transistor having a memory cell structure pull-down transistor first flow electrode, a memory cell structure pull-down transistor second flow electrode, and a memory cell structure pull-down transistor control electrode;

a logic gate operatively coupled to said memory cell structure pull-down transistor control electrode;

a memory cell operatively coupled to said logic gate; and

a supply voltage operatively coupled to said memory cell structure pull-down transistor second flow electrode;

at least one write word line operatively coupled to said memory cell of said at least one memory cell structure;

at least one read word line operatively coupled to said logic gate of said at least one memory cell structure;

at least one read bit line operatively coupled to said first flow electrode of said memory cell structure pull-down transistor of said at least one memory cell structure; and

a corruption prevention circuit operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit forces said at least one read bit line to a known digital value.

11. The improved memory structure of Claim 10, wherein;

said known digital value is a digital low value.

12. The improved memory structure of Claim 11, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

13. The improved memory structure of Claim 12, wherein;

said corruption prevention circuit comprises:

a corruption prevention circuit pull-down transistor, said corruption prevention circuit pull-down transistor having a corruption prevention circuit pull-down transistor first flow electrode, a corruption prevention circuit pull-down transistor second flow electrode, and a corruption prevention circuit pull-down transistor control electrode, said corruption prevention circuit pull-down transistor first flow electrode being coupled to said at least one read bit line, said corruption prevention circuit pull-down transistor second flow electrode being coupled to said supply voltage, said corruption prevention circuit pull-down transistor control electrode being coupled to said write word line.

14. The improved memory structure of Claim 10, wherein;

said memory structure is a rotated-read register file.

15. The improved memory structure of Claim 14, wherein;

said known digital value is a digital low value.

16. The improved memory structure of Claim 15, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

17. The improved memory structure of Claim 16, wherein;

said corruption prevention circuit comprises:

a corruption prevention circuit pull-down transistor, said corruption prevention circuit pull-down transistor having a corruption prevention circuit pull-down transistor first flow electrode, a corruption prevention circuit pull-down transistor second flow electrode, and a corruption prevention circuit pull-down transistor control electrode, said corruption prevention circuit pull-down transistor first flow electrode being coupled to said at least one read bit line, said corruption prevention circuit pull-down transistor second flow electrode being coupled to said supply voltage, said corruption prevention circuit pull-down transistor control electrode being coupled to said write word line.

18. The improved memory structure of Claim 10, wherein;

said memory structure is a Content Addressable Memory array.

19. The improved memory structure of Claim 18, wherein;

said known digital value is a digital low value.

20. The improved memory structure of Claim 19, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure

during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

21. The improved memory structure of Claim 20, wherein;

said corruption prevention circuit comprises:

a corruption prevention circuit pull-down transistor, said corruption prevention circuit pull-down transistor having a corruption prevention circuit pull-down transistor first flow electrode, a corruption prevention circuit pull-down transistor second flow electrode, and a corruption prevention circuit pull-down transistor control electrode, said corruption prevention circuit pull-down transistor first flow electrode being coupled to said at least one read bit line, said corruption prevention circuit pull-down transistor second flow electrode being coupled to said supply voltage, said corruption prevention circuit pull-down transistor control electrode being coupled to said write word line.

22. A method for preventing corruption of data in a memory structure comprising:

providing a memory structure, said memory structure comprising at least one memory cell structure;

operatively coupling at least one write word line to said at least one memory cell structure;

operatively coupling at least one read word line to said at least one memory cell structure;

operatively coupling at least one read bit line to said at least one memory cell structure; and

operatively coupling a corruption prevention circuit to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit forces said at least one read bit line to a known digital value.

23. The method for preventing corruption of data in a memory structure of Claim 22, wherein;
said known digital value is a digital low value.

24. The method for preventing corruption of data in a memory structure of Claim 23, wherein;
said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

25. The method for preventing corruption of data in a memory structure of Claim 22, wherein;
said memory structure is a rotated-read register file.

26. The method for preventing corruption of data in a memory structure of Claim 25, wherein;
said known digital value is a digital low value.

27. The method for preventing corruption of data in a memory structure of Claim 26, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.

28. The method for preventing corruption of data in a memory structure of Claim 22, wherein;

said memory structure is a Content Addressable Memory array.

29. The method for preventing corruption of data in a memory structure of Claim 28, wherein;

said known digital value is a digital low value.

30. The method for preventing corruption of data in a memory structure of Claim 29, wherein;

said corruption prevention circuit is operatively coupled to said at least one write word line and said memory cell structure such that when a read operation is enabled for said at least one memory cell structure during a write operation for said at least one memory cell structure, said corruption prevention circuit causes said read bit line to be discharged.